

A/D interface for PLC 2 inputs for V or mA

DAT 6013

FEATURES

- Analog Signal Acquisition on PLC digital I/O
- Analog Input to any PLC, even microPLC
- Isolated to eliminate Ground Loops
- 16-bits resolution with high F.S. accuracy
- V or mA input
- 2 analog inputs operation
- 12.5 mm. thin profile housing

APPLICATIONS

- Factory Automation
- Building Automation
- Agricolture Automation
- Chemical Industry Measurement
- Security system
- . Machine Control



GENERAL INFORMATION

The DAT6000 series is an evolution in the connection techniques of the analog signals to the PLC.

The devices of this Serie perform many functions such as: amplification, linearization, isolation, filtering and conversion of analog signals coming from various types of sensors, in a high resolution digital signal. The digital signal is transfered to the PLC by a bus connected at any one of controller's digital inputs. It is composed by a series of 16-bit 'words' containing the values of the analog signals to be measured. The transfer is PLC controlled by a clock signal coming from one its output ports. The query of device is made supplying to it an enabling signal (ENABLE) and a clock signal (CLK). If the ENABLE is high, a bit composing the reading is provided on the output (DATA) at every clock pulse.

Few and simple instructions loaded into the PLC enable it to acquire up to two analog signals on a single digital input.

Every reading cycle is composed of 1 synchronism bit followed of a 16 bit word for each analog input signal (channel). So each reading is composed of 33 bits. The rising front of the ENABLE signal, handled by the controller, resets the reading cycle, avoidind the reading of unused channels. The Enable signal can be used also to "multiplexing" more devices to the same digital input of the PLC.

The DAT6013 module, designed, manufactured and tested in strict accordance with the quality assurance standard UNI EN ISO 9001:2000, is in compliance with the directive 89/336/EEC on the electromagnetic compatibility and the CE mark confirms its compliance. The device is housed in a rough self estinguishing plastic container which, thank to its thin profile of 12.5 mm only, allows a high density mounting on DIN rail.

TECHNICAL SPECIFICATIONS (Typical @25°C and in the nominal conditions)

ANALOG INPUT Channels: Input type: Calibration Accuracy: Linearity: Input Impedance Thermal drift Lead wire influence Sampling rate Band width	2 inputs for V or mA ± 10 V and ± 20mA ±0.05% of F.S. ±0.1% of F.S. > 1 MOhm for V ; 47 Ohm for mA ±0.005 % F.S. /°C < 0.8 uV/Ohm 10 samp./sec 4 Hz
DIGITAL INTERFACE Voltage on terminals: ON state: Input impedence (ENABLE, CLK): Output's minimum load (DATA): Maximum Clock's signal frequency: Rise time (Tr)	24 Vdc typical (30 Vdc max.) >9 Vdc 4.7 KOhm 560 Ohm 500 Hz <0.2 ms
SUPPLY Supply voltage Supply current Reverse polarity protection 3-way isolation Electromagnetic Compatibility (EMC) Operating temperature Storage temperature Relative humidity(not condensing) Dimensions(W x H x T) in mm. Weight	18 \div 30 Vdc 35 mA @ 24 Vdc 60 Vdc max. 2000 Vac, 50 Hz, 1 min. In compliance with EN50081-2 and EN50082-2 - 10 \div 60 °C - 40 \div 85 °C 0 \div 90 % 90 x 98 x 12.5 mm 50 g. approx.

INPUT TYPES AND RANGES

Voltage			Current		
Input	Min	Max	Input	Min	Max
10 V	-10 V	+10 V	20 mA	-20 mA	+20 mA

OPERATING INSTRUCTIONS

To put the device in operation it is necessary to make the wiring of power supply, analog input and the digital output to the controller as indicated in the "BLOCK DIAGRAM" hereafter illustrated.

The device can be configured via dip-switch (SW1..SW3); so it is possible to set 2 different input types, as shown in the table below. Both the inputs have the same configuration. Consequently the input signals must be of the same type.

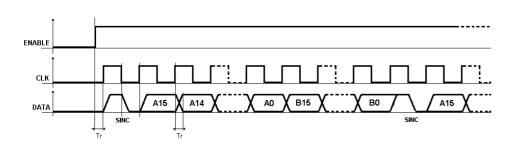
Also the CLK signal's digital filter, can be set to 1ms or 10ms (half-period duration) by a dip-switch (SW4).

The above described setting can be defined at the order phase, getting a module already set to work; otherwise the device is supplied in compliance to the following settings:

Input : 10V / Digital Filter : 1ms

DATAREADING

DIP-SWITCH CONFIGURATION



BLOCK DIAGRAM

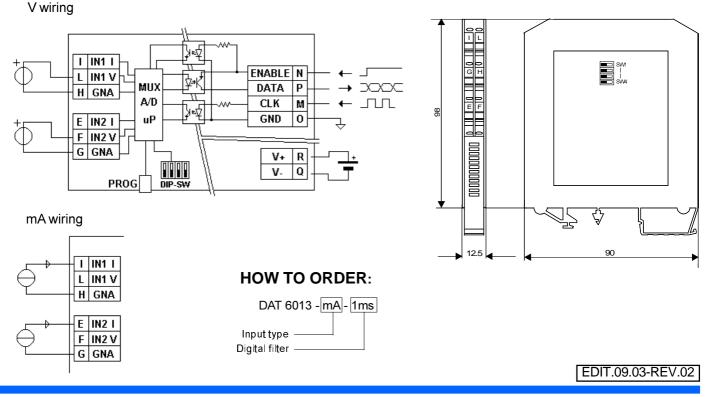
SW3	SW2	SW1	Input			
0	0	0	10 V			
0	0	1	20 mA			
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				
SW4	Digital Filter (CLK)					

1 ms (500 Hz)

10 ms (50 Hz)

MECHANICAL DIMENSIONS (mm.)

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